R22 Regulation *Subject code:4P6DA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Regular/Supplementary Examinations, April 2026

DIGITAL DESIGN THROUGH VERILOG HDL

(ECE)

Maximum Marks: 60 Date:21.04.2026 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X1M=10 Marks)		Marks	CO	Bloom Tx
1.a)	Explain in brief the role of Verilog HDL in ASIC Design.	1M	1	L2
b)	List the logic level strengths in decreasing order of their values	1M	1	L1
c)	List the types of gate primitives available in Verilog HDL	1M	2	L1
d)	Write an XOR gate primitive expression with a positive – negative delay to be 1 time step and negative – positive delay to be 3 - time steps.	1M	2	L2
e)	Give the example usage of delays with continuous assignment along with timing diagram.	1M	3	L2
f)	Draw the circuit diagram of a 2 – input CMOS NOR Gate	1M	3	L2
g)	What is non - blocking assignment? Give an example.	1M	4	L1
h)	Differentiate for and while loops.	1M	4	L2
i)	Define functions in Verilog HDL.	1M	5	L1
j)	Differentiate combinational and sequential UDPs.	1M	5	L2

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	Bloom Tx
2	a) Explain the lexical tokens present in Verilog along with examples. b) Define concurrency. How does it differ from sequential programming languages?	5M 5M	1	L1 L2
	OR			
3	a) Explain the conventional approach to digital design. b) Explain different levels of design description.	5M 5M	1	L2 L1
4	a) Design an 8 – bit ALU using Gate level modelling along with test bench. b) Design a 4x1 multiplexer using tri – state gates.	6M 4M	2	L3 L3
	OR			
5	a) Design a 3x8 Decoder using two 2x4 decoders. Also write a test bench for the same. b) Differentiate Net delays and Gate delays.	5M 5M	2	L3 L2

6	a) What is a CMOS switch? Realize a CMOS switch using NMOS and PMOS transistors. b) Explain the operators present in Verilog HDL in detail with examples.	5M 5M	3	L2 L2
	OR			
7	a) Design - i) 4x1 multiplexer ii) 1x4 demultiplexer using conditional operators. Write test benches for the same. b) Explain Bi – Directional gates with examples.	5M 5M	3	L3 L2
8	a) Design a 8-bit universal shift register with the following capabilities i) Shift right ii) Shift left iii) Rotate right iv) Rotate left. Test the same using a test bench. b) Realize a 3x8 priority encoder using "casex" construct.	7M 3M	4	L3 L3
	OR			
9	a) Design a SR flip flop with an asynchronous active high reset. b) Explain conditional statements in Verilog HDL.	5M 5M	4	L3 L2
10	a) Write a UDP for a D – Flip Flop and test the same through a test bench. b) Explain compiler directives with examples.	6M 4M	5	L3 L2
	OR			
11	a) Differentiate Functions, UDPs and Tasks. b) Explain about parameters with an example.	5M 5M	5	L2 L3

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